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Statistical real-time communication over Ethernet for manufacturing automation systems

- Seok-Kyu Kweon; Shin, K.G.; Zin Zheng

Dept. of Electr. Eng. & Comput. Sci., Michigan Univ., Ann Arbor, MI, USA

This paper appears in: Real-Time Technology and Applications Symposium Proceedings of the Fifth IEEE

On page(s): 192 - 202

2-4 June 1999

1999

ISBN: 0-7695-0194-X

Number of Pages: xi+293

References Cited: 10

INSPEC Accession Number: 6325305

Abstract:

In order to realize real time communication over Ethernet or fast Ethernet, on able to bound the medium access time within an acceptable limit. The multiple nature of an Ethernet makes it impossible to guarantee a deterministic medium time to individual stations. However one can bound the medium access time s by limiting the packet arrival rate at the medium access control (MAC) layer. W focusing on automated manufacturing systems as the main application, the pa considers the connection admission control (CAC) problem for statistically bou medium access time of Ethernet. Specifically, a packet is guaranteed to have access time smaller than a predefined bound with a certain probability if the instantaneous packet arrival rate is kept below a certain threshold. Through a we first derived such a threshold. In order to keep the packet arrival rate unde given threshold, we employ a traffic smoother which: (i) is located between th transport layer and the Ethernet datalink layer and (ii) smooths packet stream the two layers. The implementation of this traffic smoother requires only a mi change in the OS kernel without any modification to the current standard of E MAC protocol or TCP or UDP/IP stack. In order to solve the CAC problem, we d probability of transmitting a packet successfully upon each trial by modeling t protocol, 1-persistent CSMA/CD, and the collision resolution protocol, Binary E Backoff, of Ethernet. We implemented a traffic smoother on the Linux OS, dem the effectiveness of our approach in providing real time communication over E

Index Terms:

local area networks; statistical real time communication; manufacturing autom systems; fast Ethernet; medium access time; deterministic medium access tim arrival rate; medium access control layer; automated manufacturing systems; connection admission control; instantaneous packet arrival rate; traffic smoot transport layer; Ethernet datalink layer; packet streams; OS kernel; Ethernet protocol; TCP; UDP/IP stack; CAC problem; probability; MAC protocol; 1-persi CSMA/CD; collision resolution protocol; Binary Exponential Backoff; Linux OS

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This paper appears in: IEEE Std 802.11b-1999

On page(s): i - 90

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ISBN: 0-7381-1811-7

Abstract:

Changes and additions to IEEE Std 802.11, 1999 Edition are provided to support higher rate physical layer (PHY) for operation in the 2.4 GHz band.

Index Terms:

2.4 GHz, high speed, local area network (LAN), radio frequency (RF), wireless

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Instruction-Driven Wake-Up Mechanisms for Snoopy TAP Controller

Debashis Bhattacharya
Texas Instruments Incorporated

The issue of handling multiple embedded 1149.1-compliant TAP controllers (as part of embedded cores) in a 1149.1-compliant IC, has received significant attention, in recent times. The Hierarchical TAP (HTAP) architecture, previously developed by this author, provides a systematic solution to this problem, by allowing multiple embedded TAP's to share one set of 1149.1-specified test pins on the IC. The HTAP architecture requires an augmented version of the 1149.1-specified TAP - designated the *Snoopy TAP (SNTAP)* - in the top-level of the design hierarchy, that handles 1149.1-specified TAP functions for the non-TAP'ed parts of the IC, and performs arbitration of the shared IC pins between multiple embedded TAPs. Previously, a mechanism was developed to *wake up the SNTAP* using a simple string of constant values (0 or 1) on the TMS input. Two new mechanisms to wake up SNTAP by means of an instruction scanned in, are described in this report. Both mechanisms allow embedded 1149.1-compliant TAP's to be used in a hierarchical design, as is, without any hardware modification. Moreover, both mechanisms enable reuse of the test program from the embedded TAP'ed cores, without any modification. The instructions to wake up the SNTAP - to switch access to different TAP-ed cores - can be simply inserted in-between the test programs for the embedded cores.

Proceedings of the 1999 17TH IEEE VLSI Test Symposium
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Hardware monitoring of a multiprocessor system

- Liu, A.-C.; Parthasarathi, R.

Feng Chia Univ., Taichung, Taiwan

This paper appears in: IEEE Micro

On page(s): 44 - 51

Oct. 1989

Volume: 9 Issue: 5

ISSN: 0272-1732

References Cited: 8

CODEN: IEMIDZ

INSPEC Accession Number: 3547387

Abstract:

The Testbed for Distributed Processing, or Ted, consists of Intel Corp.'s iSBC 8 board computers (SBCs) organized into groups or clusters. Each cluster consists of several SBCs that communicate via a shared memory. Intercluster communication occurs through an Ethernet interface. A hardware monitor designed and implemented to handle the monitoring activities within a cluster in the Ted system is described. Specified patterns and don't-care masks, the system can detect accesses to specific data, addresses, or blocks of addresses. This function helps monitor events such as access or usage of a memory location or a group of mailbox addresses. It also determines the amount of time consumed by the performance of specific operations.

Index Terms:

hardware monitoring; intercluster communication; multiprocessor system; Testbed for Distributed Processing; Ted; iSBC 8086 single board computers; Ethernet interface; addresses; blocks of addresses; memory location; mailbox addresses; multiprocessor systems; performance evaluation

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